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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,354	07/07/2003	Thomas J. Sonderman	2000.100800	7900

23720 7590 06/21/2005

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EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,354	SONDERMAN ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,6-9,11-15,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6-9,11-15,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

New Grounds of Rejection

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 6-9, 11-15, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (U.S. Patent 5,793,675) in view of Wong (U.S. Patent 6,882,567).

In re claims 1, 9, and 16, **Cappelletti** discloses a method, comprising: performing at least one electrical test (i.e., threshold voltage…) on at least one flash memory device (col. 2, lines 21-28) (memory device, transistor) (col. 3, lines 12-46);

determining at least one parameter (i.e., temperature…) of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed flash memory device (i.e., memory device, transistor…) based upon electrical data obtained from the at least one electrical test (col. 3, lines 48-59); and

performing the at least one process operation comprised of the determined at least one parameter to form at least one gate insulation layer on the subsequently formed flash memory device (memory device, transistor) (col. 5, lines 27 to col. 6, line 16).

Cappelletti discloses performing at least one electrical test on at least one flash memory device to determine a threshold voltage (col. 3, line 12-46) but does not

explicitly disclose that performing at least one electrical test on at least one flash memory device to determine a duration of a programming cycle performed on the flash memory device as required in independent claim 1 and to determine a duration of an erase cycle performed on the flash memory device as recited in independent claim 9.

Wong, however, provides evidence that there is a relationship between the threshold voltage and the duration of a programming cycle (col. 14, lines 25-39) and in addition, the relationship between the threshold voltage and the duration of an erase cycle. Therefore, to perform at least one electrical test on a flash memory device to determine a threshold voltage inherently determine the duration of a programming cycle and the duration of an erase cycle performed on the flash memory device. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Cappelletti and Wong to enable the process of performing at least one electrical test on at least one flash memory device to determine a duration of a programming cycle and a duration of an erase cycle performed on the flash memory device of Cappelletti to be performed and furthermore to achieve uniform programming accuracy across a range of target threshold voltages (Abstract, Wong).

In re claims 3 and 11, **Cappelletti** discloses that performing the at least one electrical test on the at least one flash device further comprises performing the at least one electrical test on the at least one flash memory device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, and an erase cycle time (col. 3, lines 16-46).

In re claim 12, **Cappelletti** discloses that the semiconductor device is comprised of a memory device that is comprised of a gate insulation layer 4, a floating gate layer 5 positioned above the gate insulation layer 4, an intermediate insulation layer 6 positioned above the floating gate layer 5, and a control gate layer 7 positioned above the intermediate insulation layer 6 (col. 1, lines 18-27 and FIG. 1).

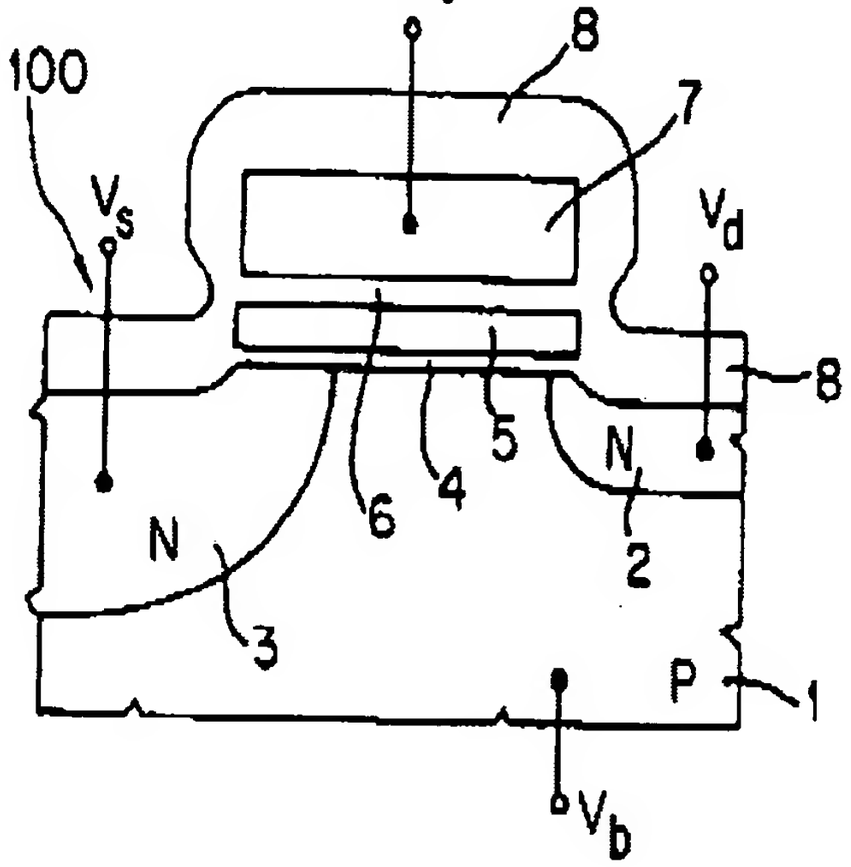

FIG. 1
PRIOR ART

In re claims 6 and 13, the technique of performing the at least one process operation to form the at least one gate insulation layer on the subsequently formed semiconductor device comprises of at least one of a deposition process and a thermal growth process is well-known to one of ordinary skill in the art at the time of the invention was made.

In re claims 7 and 14, **Cappelletti** discloses that at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate,

a process gas composition, a liquid flow rate, a liquid composition, and a power level setting (col. 3, lines 16-59).

In re claims 8 and 15, **Cappelletti** discloses that the gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride (col. 1, lines 18-28).

In re claims 21 and 22, **Cappelletti** discloses a method, comprising: performing at least one electrical test on at least one memory device to determine a threshold voltage performed on the memory devices (col. 3, lines 12-46 and col. 4, line 66 to col. 5, line 13);

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon the determined duration of the programming cycle (col. 3, lines 48-59); and

performing the at least one process operation comprised of the determined at least one parameter to form at least one gate insulation layer on the subsequently formed memory device (col. 5, lines 27 to col. 6, line 16).

Cappelletti discloses performing at least one electrical test on at least one flash memory device to determine a threshold voltage (col. 3, line 12-46) but does not explicitly disclose that performing at least one electrical test on at least one flash memory device to determine a duration of a programming cycle performed on the flash memory device as required in independent claim 21 and to determine a duration of an erase cycle performed on the flash memory device as recited in independent claim 22.

Wong, however, provides evidence that there is a relationship between the threshold voltage and the duration of a programming cycle (col. 14, lines 25-39) and in addition, the relationship between the threshold voltage and the duration of an erase cycle. Therefore, to perform at least one electrical test on a flash memory device to determine a threshold voltage inherently determine the duration of a programming cycle and the duration of an erase cycle performed on the flash memory device. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Cappelletti and Wong to enable the process of performing at least one electrical test on at least one flash memory device to determine a duration of a programming cycle and a duration of an erase cycle performed on the flash memory device of Cappelletti to be performed and furthermore to achieve uniform programming accuracy across a range of target threshold voltages (Abstract, Wong).

Response to Applicant's Amendment and Arguments

Applicant's arguments with respect to claims 1, 3, 6-9, 11-15, and 21-22 have been considered but are moot in view of the new ground(s) of rejection.

Applicants contend that at no point does Cappelletti disclose nor suggest performing at least one electrical test to determine the duration of a programming cycle of a flash memory device or to determine the duration of an erase cycle for a flash memory device.

In response to Applicants' contention that at no point does Cappelletti disclose nor suggest performing at least one electrical test to determine the duration of a programming cycle of a flash memory device or to determine the duration of an erase

cycle for a flash memory device. Since Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action, Examiner respectfully submits that Applicants' argument is moot in view of the newly discovered reference to Wong (U.S. Patent 6,882,567) applied under 35 U.S.C. 103(a) rejection presented in this Office Action (See, page 2, 2nd paragraph to page 3, 1st paragraph of this Office Action). For this reason, Examiner holds the rejection proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
June 15th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER